

FIG. 1

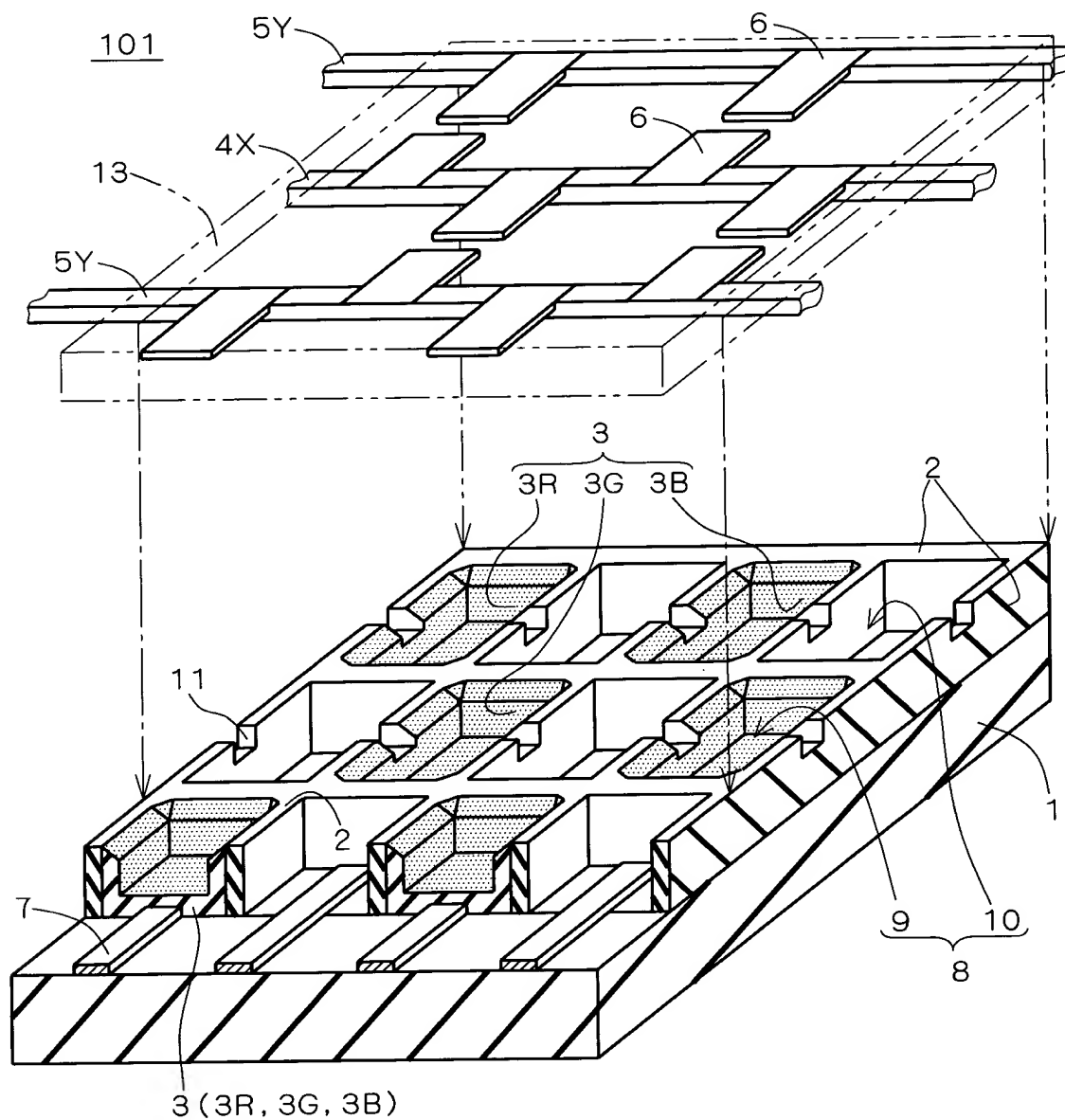


FIG. 2

101

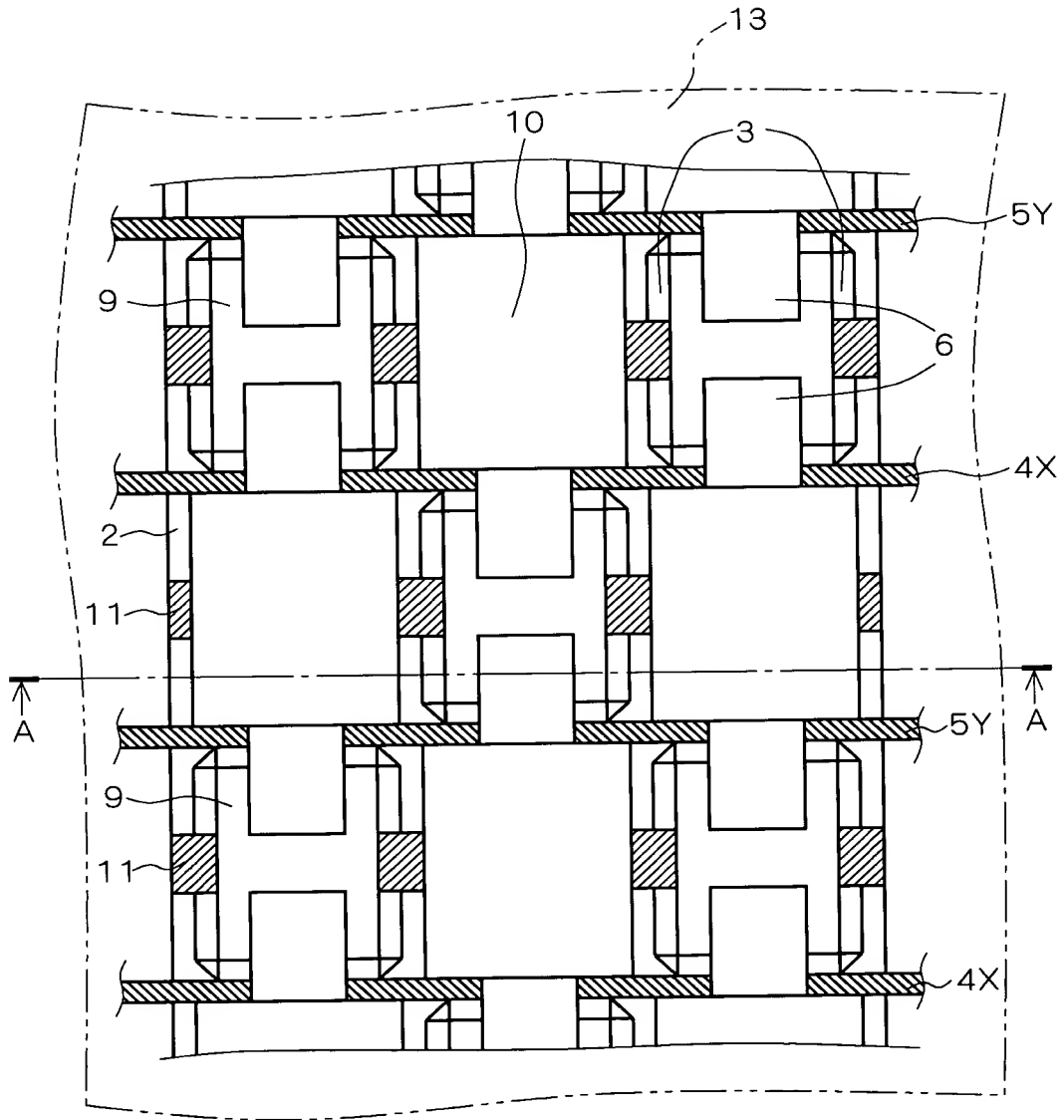


FIG. 2

FIG. 3

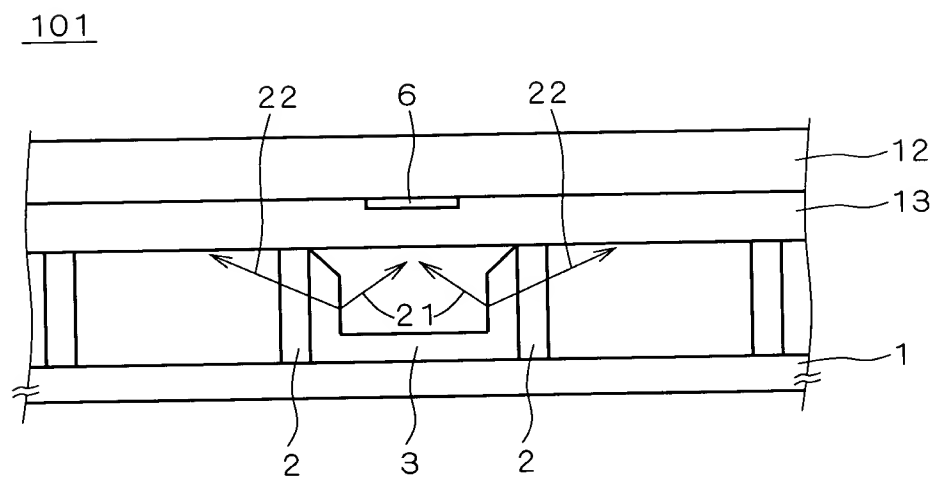


FIG. 4

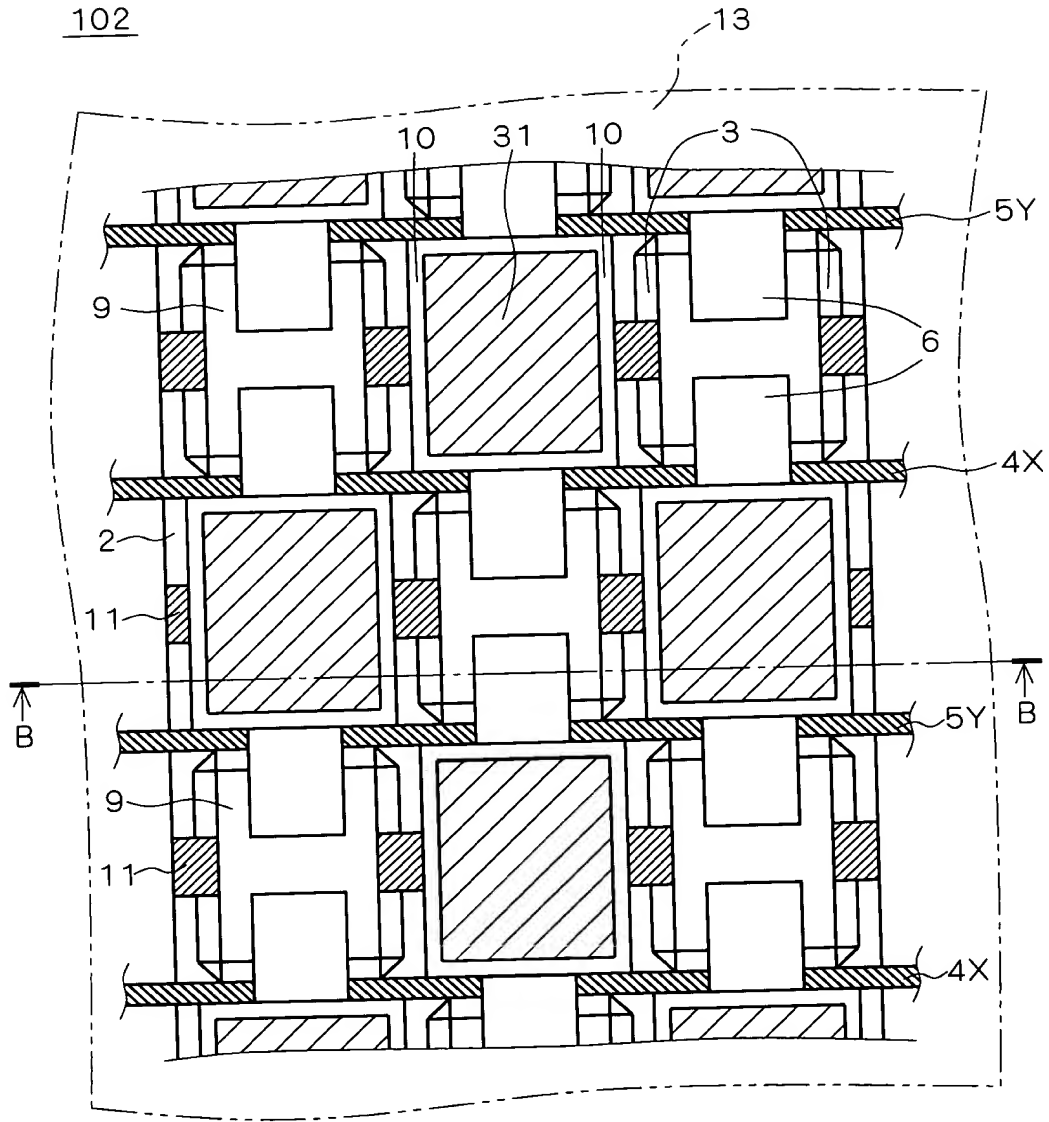


FIG. 5

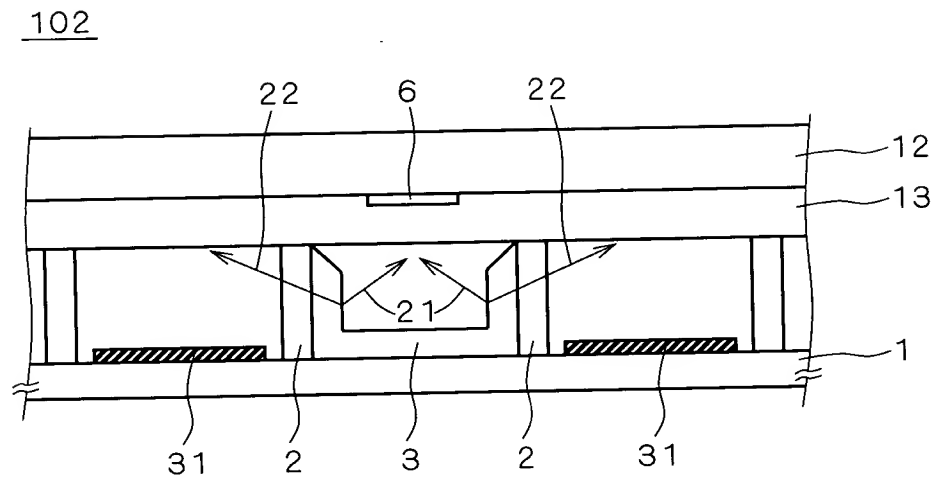
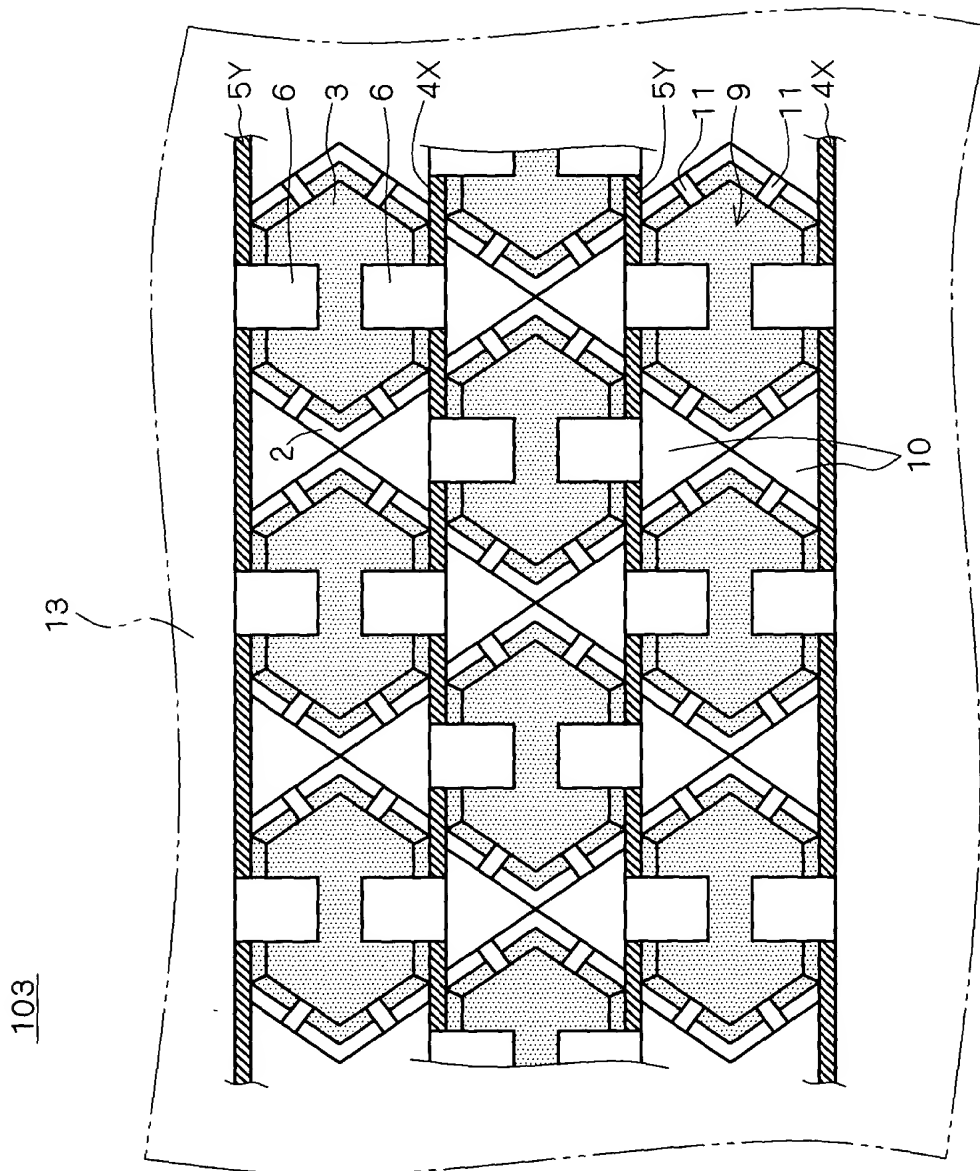


FIG. 6



103:PDP

FIG. 7

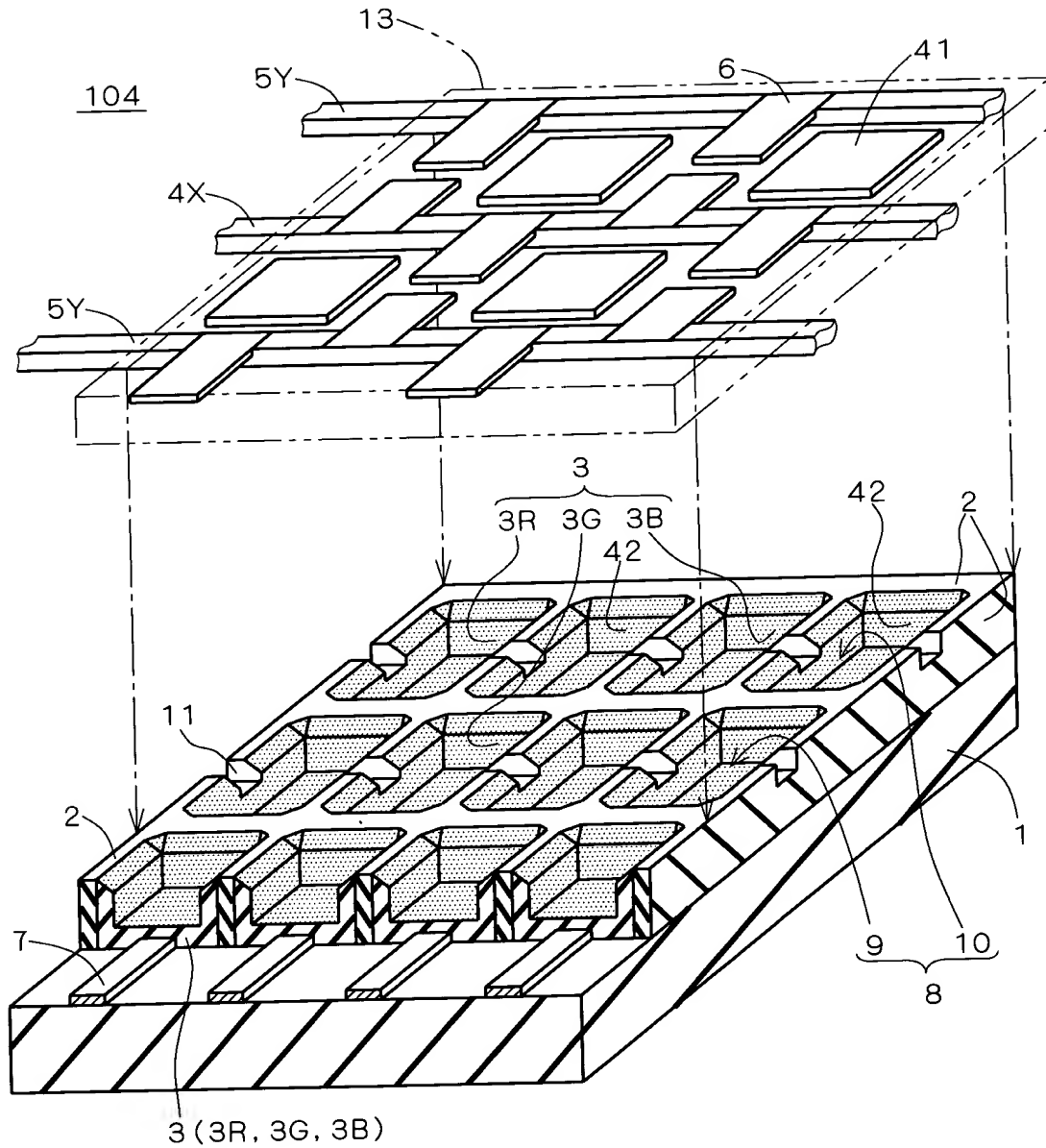
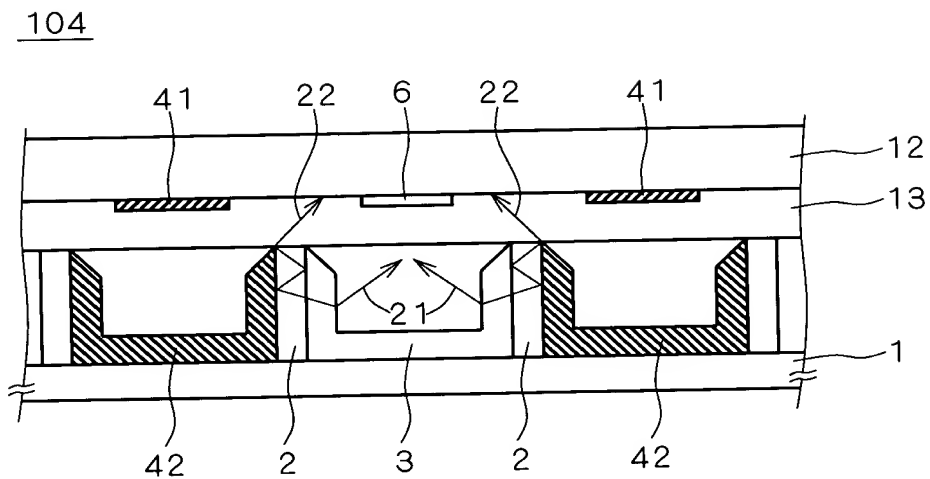


FIG. 7

FIG. 10 is a cross-sectional view of a semiconductor device, showing a 3x3 array of memory cells. The array is bounded by a dashed line 13. Each cell contains a vertical word line 41, a horizontal bit line 42, and a storage capacitor 6. The array is surrounded by a peripheral circuit 9. The device is mounted on a substrate 10. The cross-section is taken along line C-C.



$F / G. 9$



$F / G. 10$

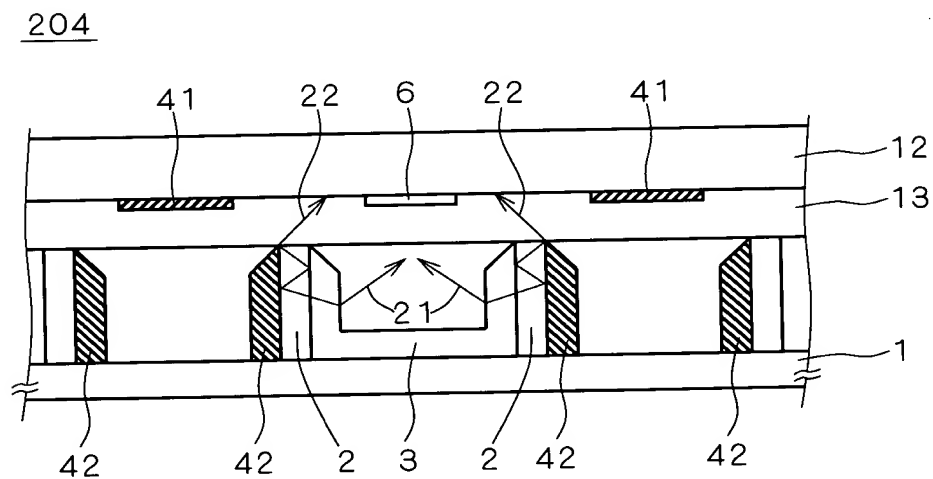


FIG. 11

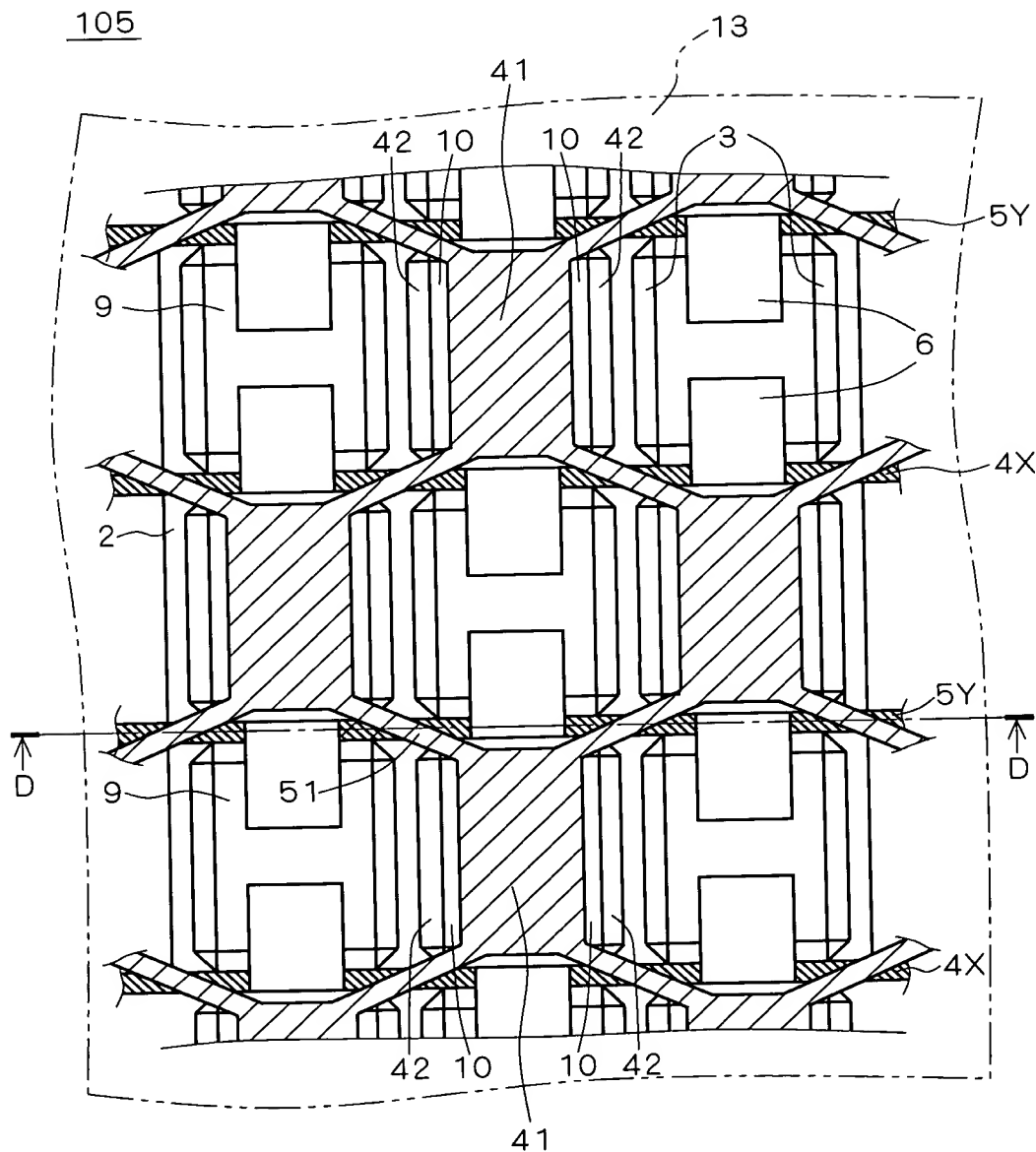
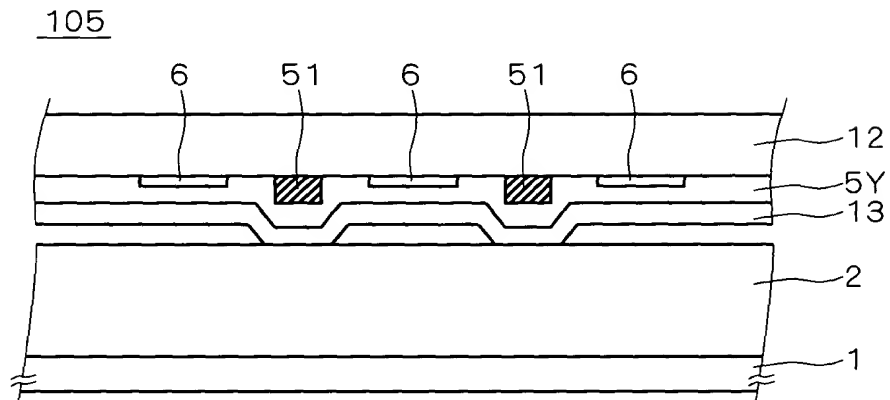


FIG. 11

*F / G. 12*



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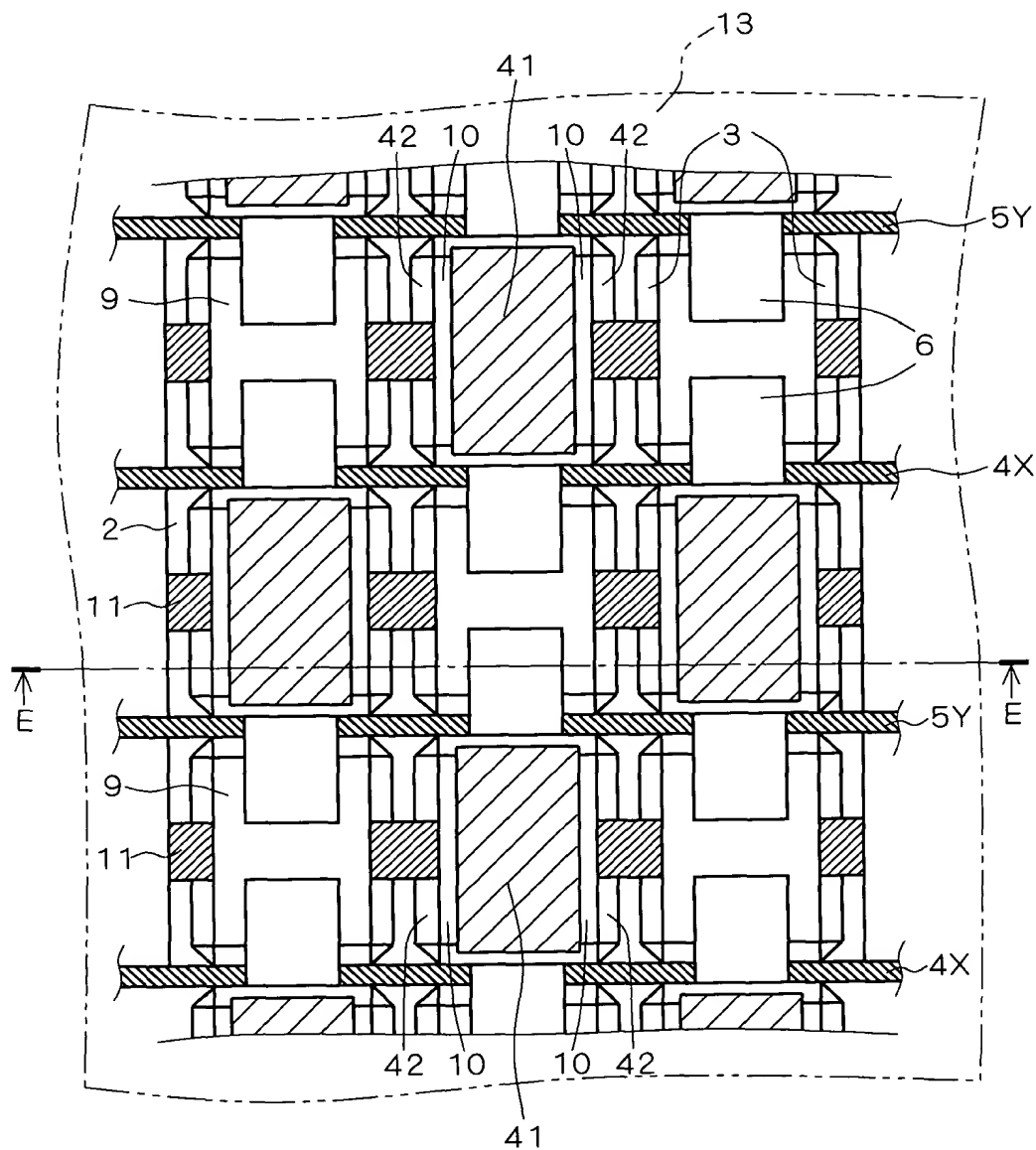


FIG. 14

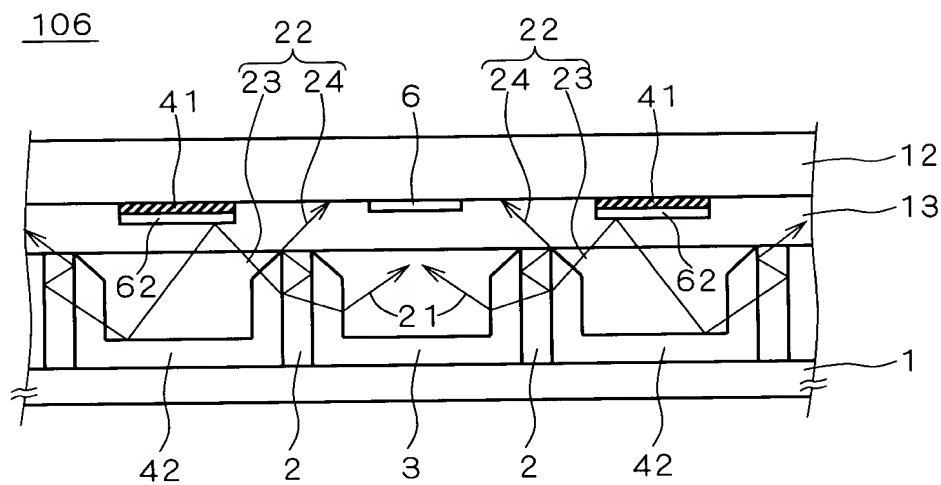


FIG. 15

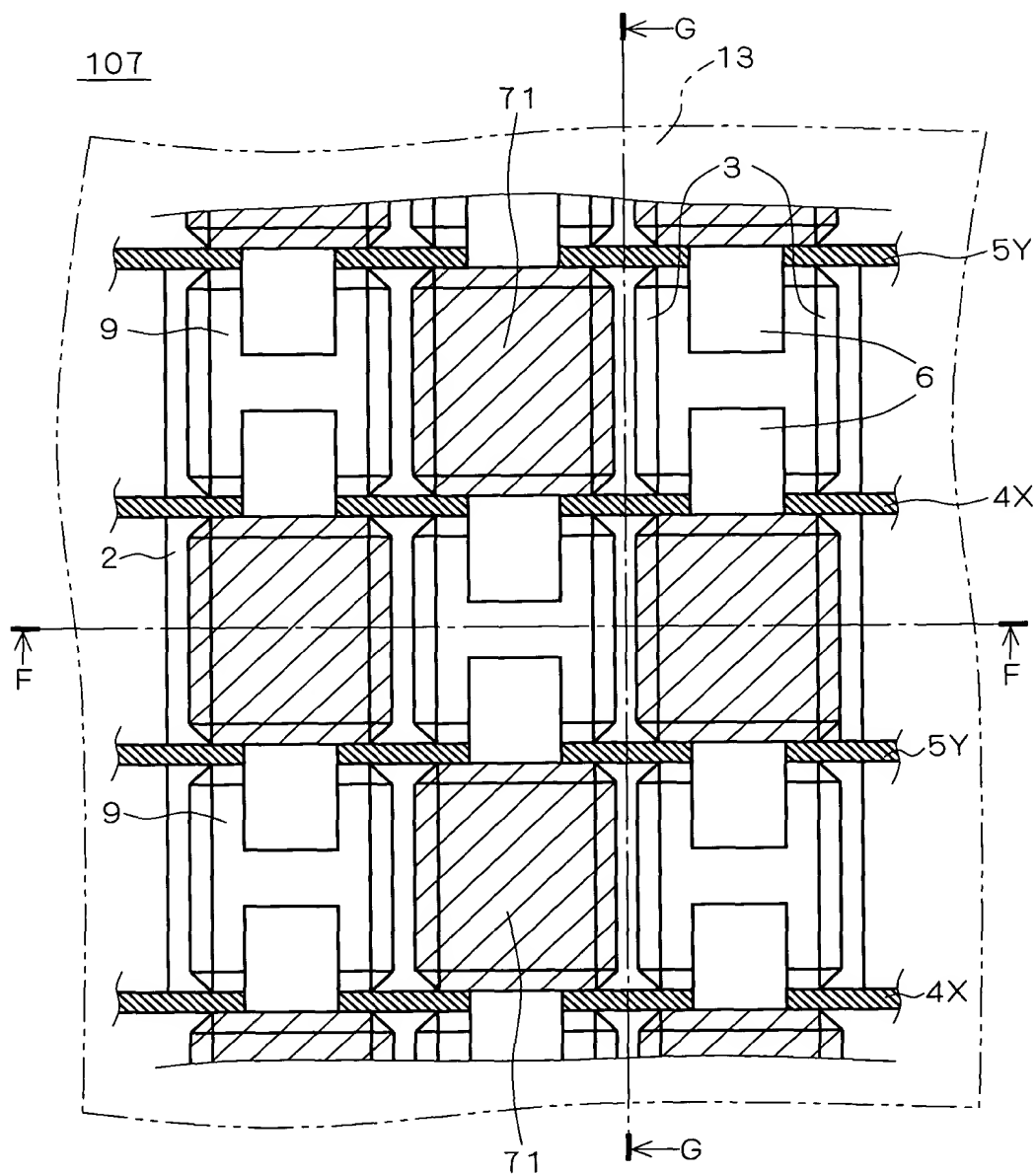


FIG. 16

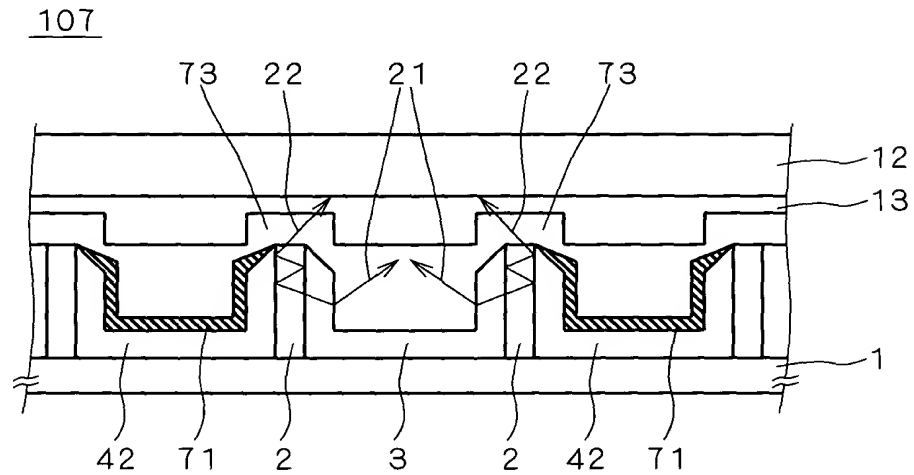


FIG. 17

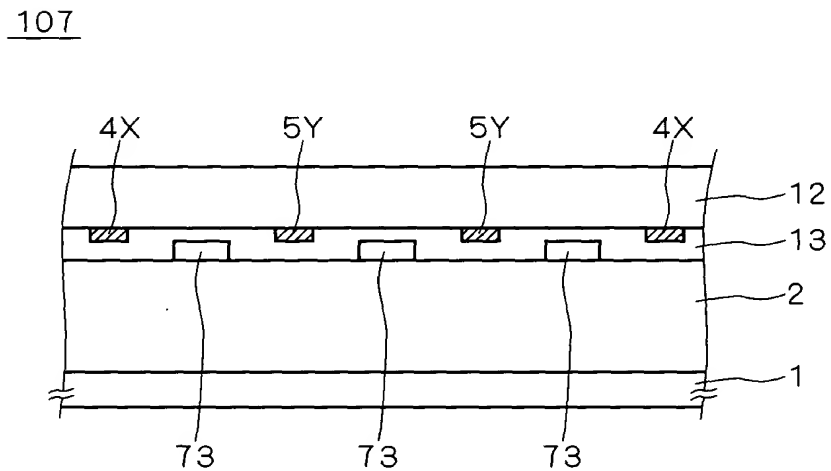


FIG. 18

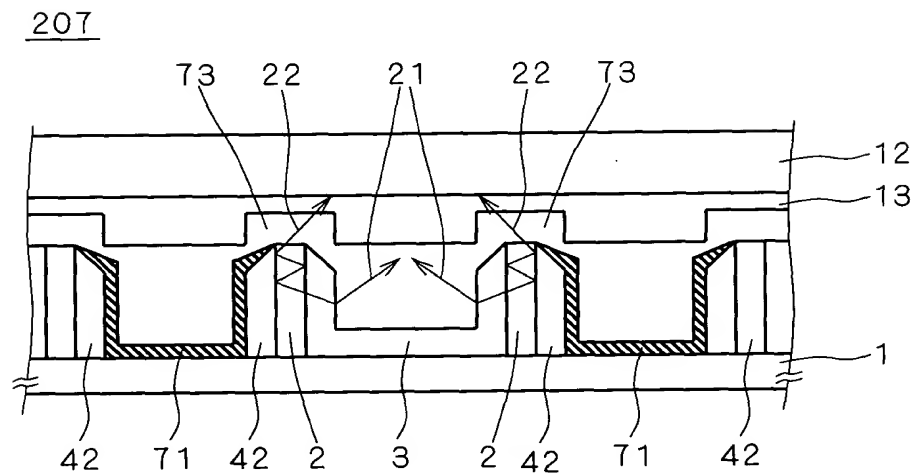




FIG. 19

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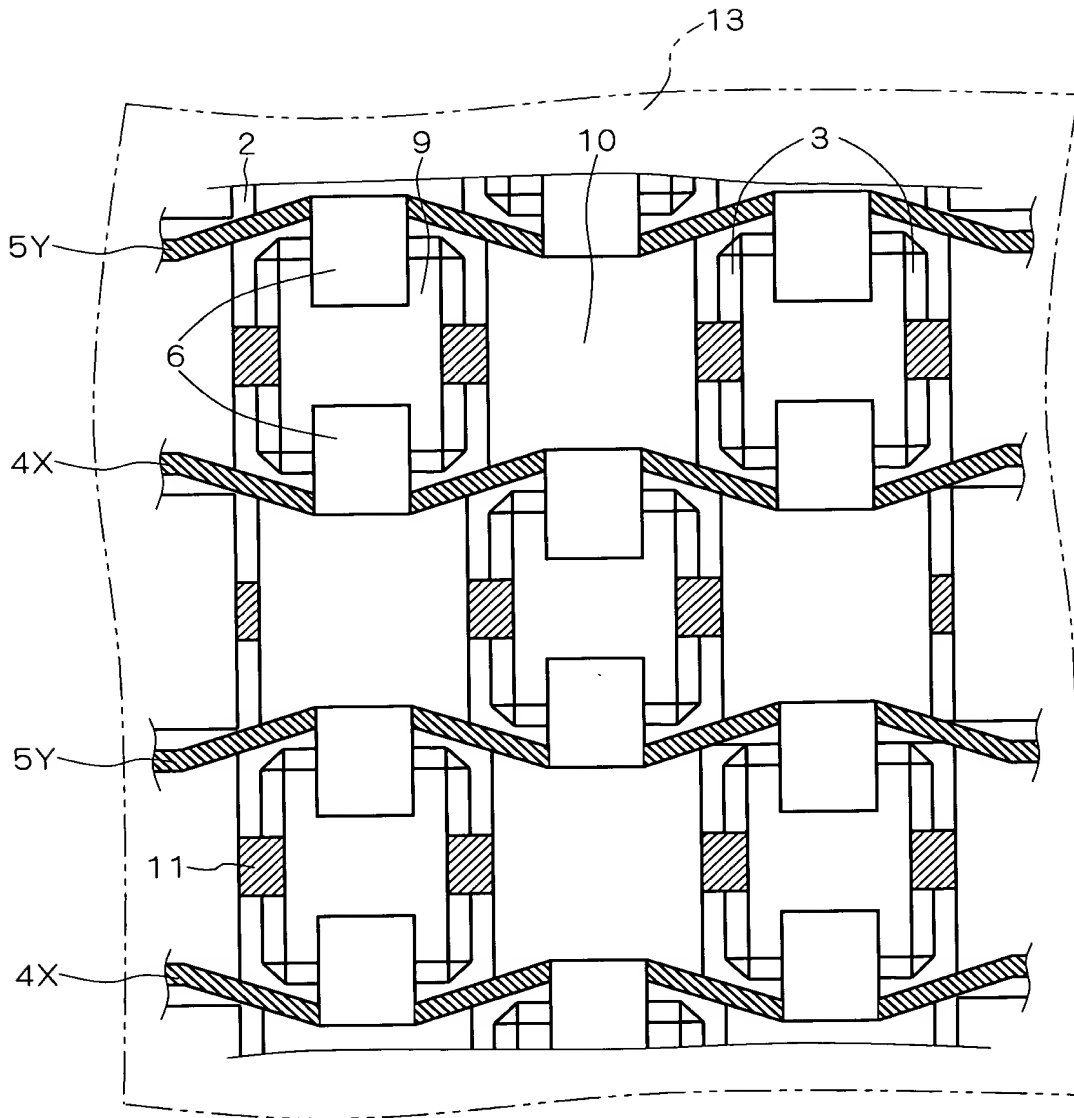


FIG. 20

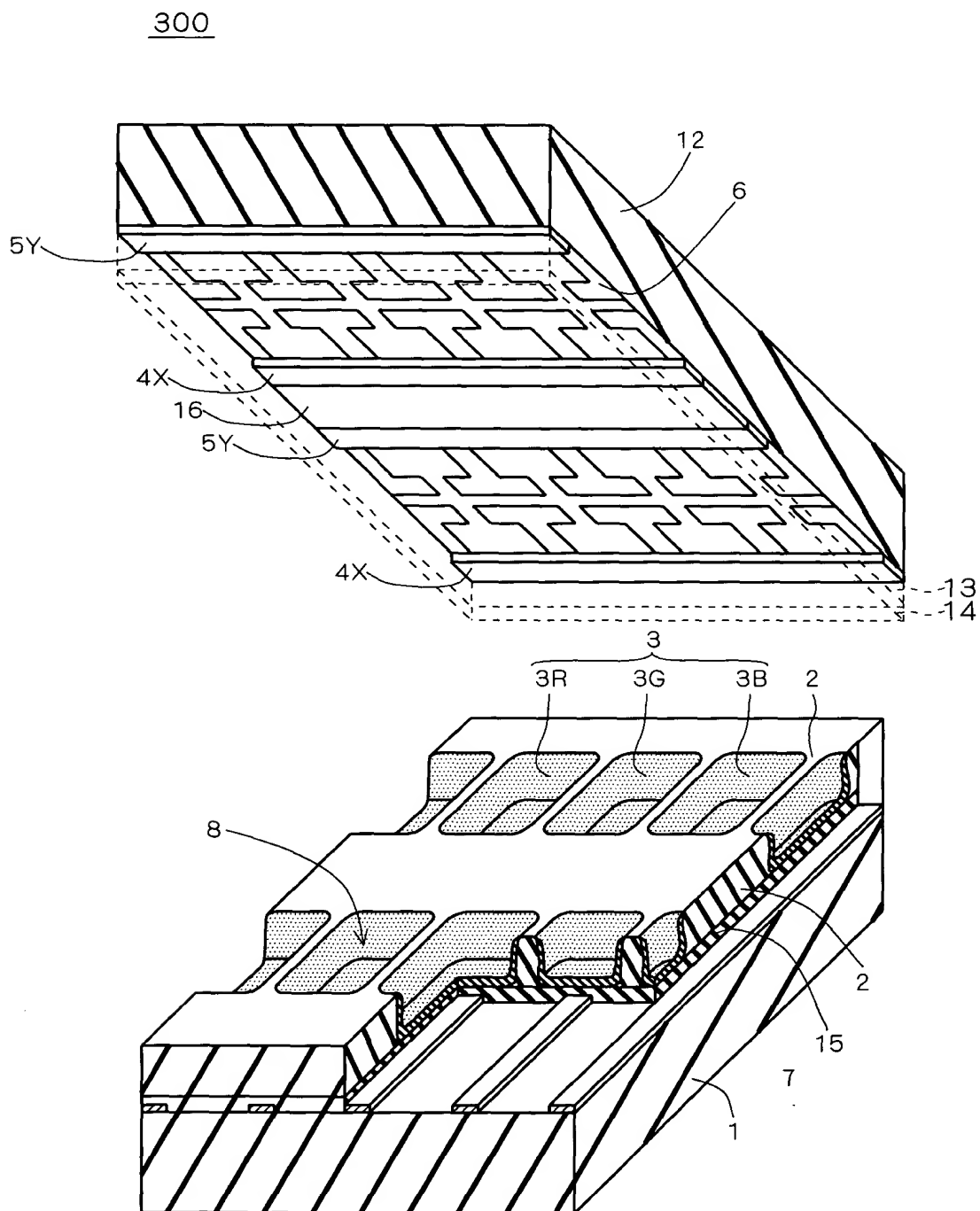


FIG. 21

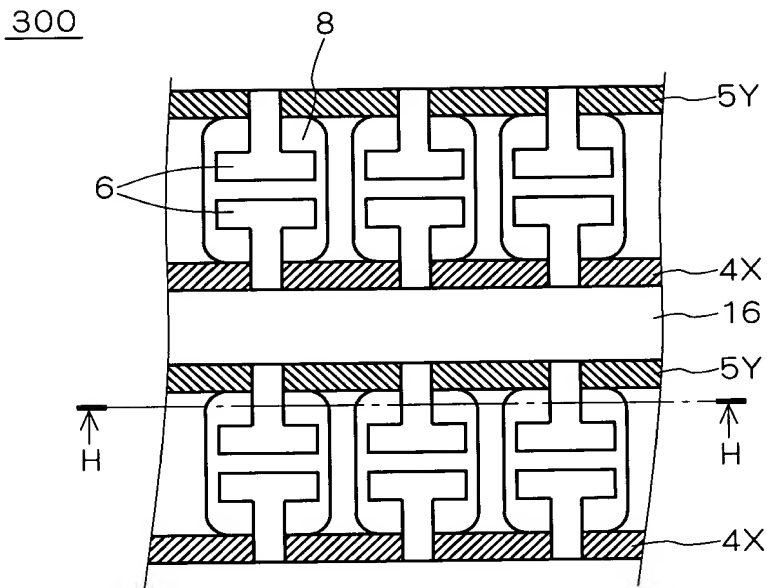


FIG. 22

